REMARKS:

This is in response to the Office Action dated September 13, 2001, which was paper #12 of the application. Applicants amend the title of the invention. Applicants amend claims 1, 3, and 15 of the application; marked up versions of the amended claims are attached hereto pursuant to 37 C.F.R. § 1.121(c)(ii). Pursuant to this amendment, claims 1-6 and 15 are pending in the application. Reexamination and reconsideration of the application are respectfully requested.

The Examiner objects to the title of the invention. Applicants amend the title of the invention to address this objection.

The Examiner rejects claims 1-2 and 15 as anticipated by U.S. Patent No. 5,811,318 to Kweon, by U.S. Patent No. 5,739,880 to Suzuki *et al*, and by U.S. Patent No. 6,201,590 to Ohta *et al*. The Examiner rejected claims 1-5 and 15 as obvious over U.S. Patent No. 5,247,375 to Mochizuki *et al* in view of U.S. Patent No. 5,187,604 to Taniguchi *et al*, U.S. Patent No. 5,748,179 to Ito *et al*, the Kweon patent, and U.S. Patent No. 5,777,702 to Wakagi *et al*. Applicants respectfully traverse these rejections for reasons stated below.

In page 5, paragraph 6, of the outstanding Office Action, the Examiner also rejects claims 1-6 and 15 as obvious over U.S. Patent No. 5,671,026 to Shiraki *et al*. The Examiner, however, does not name any secondary reference in this rejection under 35 U.S.C. 103(a). As a result, applicants respectfully request withdrawal of this rejection.

The present application describes an LCD having a plurality of pixel electrodes arranged in a matrix on a substrate and a first plurality of TFT elements respectively connected to each of the plurality of pixel electrodes as the switching elements. In addition, a second plurality of TFT elements are grouped into several driving circuits near the peripheral areas of the substrate and positioned around the display area of the LCD. According to the present application, at least a portion of one or more conductive section(s) is/are formed on the substrate to prevent deterioration of element characteristics due to the static electricity generated

during the manufacturing of the LCD device. FIGs. 1-3 of the present application illustrate a first embodiment of the present invention. In this embodiment, at least a portion of one of the wires connected to the drain driver 5 (e.g., the video data feeding wire 53, the horizontal start pulse feeding wire 52, or the horizontal clock pulse feeding wire 51) is arranged detouring around outside of the drain driver 5. ***An electric shielding wire 10 is formed at least on the detouring part of the selected wire(s) around outside of the drain driver 5.*** Accordingly, the electric shielding wire 10 will absorb the static electricity generated during the manufacturing process so that damages to the elements of the drain driver 5 can be prevented. See Application, page 12, line 25—page 13, line 25.

The electric shielding wire 10 includes wire pedestal 111 formed on the substrate 100, gate insulating film 102 covering the wire pedestal 111, injection stopper 104 formed on the gate insulating film 102, interlayer insulating film 105 covering the injection stopper 104 and the gate insulating film 102, wire 116 formed on the interlayer insulating film 105 and contacting the wire pedestal 111 via an opening, and flattening insulating film 108. See Application, page 10, line 17-page 12, line 24. As shown in FIG. 3, ***the wire 10 that provides electric shielding protection to the drain driver 5 includes a lamination structure with two conductive layers*** (wire pedestal 111 and wire 116). Moreover, no additional manufacturing step is required to form the electric shielding wire 10. Specifically, the wire pedestal 111 is formed with the gate electrode 101 and the input terminal pedestal 121 as the first conductive layer. The wire 116 is formed with the input terminal contact film 129 and the source and drain electrodes 106, 107 of the TFTs as the second conductive layer. Manufacturing costs of the LCD device, therefore, will not be increased.

The Kweon patent describes a method of manufacturing a LCD with reduced steps of the photolithography process. According to the Kweon patent, each of the switching TFTs in the LCD has a gate electrode formed by the first and second metal films 31, 33 (or 51, 53). The LCD's gate-pad connecting areas and the pad areas are also formed by the first and second metal films 31, 33 (or 51, 53). See

FIGs. 6-12, col. 4, line 55-col. 5, line 12 of the Kweon patent. The Kweon patent, however, does not describe the formation process of the LCD's driving circuits. Nor does it describe any wires, at least one of which having a lamination structure with two conductive layers, that are connected to the driving circuits of the LCD for providing driving signals. More importantly, ***the Kweon patent never describes at least a portion of one wire is positioned outside of a driving circuit and near the peripheral area of the substrate to function as an electric shielding wire***. Therefore, aspects of the present invention distinguish over the Kweon patent.

Similarly, neither the Suzuki patent nor the Ohta patent describes any wires, at least one of which having a lamination structure with two conductive layers, that are connected to the driving circuits of the LCD for providing driving signals. Moreover, both patents also do not describe at least a portion of one wire is positioned outside of a driving circuit and near the peripheral area of the substrate to function as an electric shielding wire. The present application distinguishes over the Suzuki patent and the Ohta patent.

With respect to the Mochizuki patent, the Taniguchi patent, the Ito patent, and the Wakagi patent, applicants respectfully submit that none of these patents describes at least a portion of one of the wires is positioned outside of a driving circuit and near the peripheral area of the substrate to function as an electric shielding wire. The present application, thus, distinguishes over the Mochizuki patent, the Taniguchi patent, the Ito patent, and the Wakagi patent.

Claim 1 of the present application recites, in pertinent part, "the portion of the wire being located near the peripheral area of the substrate and outside of said plurality of thin film transistors to function as an electric shielding wire". As discussed, none of the Kweon patent, the Suzuki patent, the Ohta patent, the Mochizuki patent, the Taniguchi patent, the Ito patent, and the Wakagi patent describes this limitation of claim 1. Thus, claim 1 distinguishes over the Kweon patent, the Suzuki patent, the Ohta patent, the Mochizuki patent, the Taniguchi patent, the Ito patent, and the Wakagi patent and is in condition for allowance.

Claim 2 depends on claim 1. Thus, claim 2 similarly distinguishes over the Kweon patent, the Suzuki patent, the Ohta patent, the Mochizuki patent, the Taniguchi patent, the Ito patent, and the Wakagi patent, and is in condition for allowance.

Claim 3 recites, in pertinent part, "the portion of the wire being located near the peripheral area of the substrate and outside of said plurality of driving thin film transistors to function as an electric shielding wire". As discussed, none of the Mochizuki patent, the Taniguchi patent, the Ito patent, the Kweon patent, and the Wakagi patent describes this limitation of claim 3. Thus, claim 3 distinguishes over the Mochizuki patent, the Taniguchi patent, the Ito patent, the Kweon patent, and the Wakagi patent, and is in condition for allowance.

Claims 4 and 5 depend on claim 3. Thus, claims 4 and 5 similarly distinguish over the Mochizuki patent, the Taniguchi patent, the Ito patent, the Kweon patent, and the Wakagi patent, and are in condition for allowance.

Claim 6 recites, in pertinent part, "a plurality of input terminals ... having a lamination structure comprising two or more conductive layers formed of two or more layers included in each switching thin film transistor and/or each driving thin film transistor, and situated 0.8 mm or further from the plurality of driving thin film transistors." Applicants submit that none of the Mochizuki patent, the Taniguchi patent, the Ito patent, the Kweon patent, and the Wakagi patent, describes this limitation of claim 3. Thus, claim 6 distinguishes over the Mochizuki patent, the Taniguchi patent, the Ito patent, the Kweon patent, and the Wakagi patent, and is in condition for allowance.

Claim 15 recites, in pertinent part, "at least a portion of one of said wires being located near the peripheral area of the substrate and outside of said plurality of thin film transistors to function as an electric shielding wire". As discussed, none of the Kweon patent, the Suzuki patent, the Ohta patent, the Mochizuki patent, the Taniguchi patent, the Ito patent, and the Wakagi patent, describes this limitation of claim 15. Thus, claim 15 distinguishes over the Kweon patent, the Suzuki patent,

the Ohta patent, the Mochizuki patent, the Taniguchi patent, the Ito patent, and the Wakagi patent, and is in condition for allowance.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6870 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
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Version with markings to show changes made:

1. (Twice Amended) A display apparatus having a plurality of pixels, comprising on a substrate:

a plurality of pixel electrodes corresponding to respective pixels among the plurality of pixels;

a plurality of thin film transistors, each located outside of said plurality of pixel electrodes and comprising a plurality of conductive layers, for controlling supplying of signal voltage to the plurality of pixel electrodes;

a plurality of input terminals for receiving a control signal for the signal voltage to be supplied to the plurality of thin film transistors; and

wires, at least some of said wires being connected between said plurality of thin film transistors and said plurality of input terminals for sending the signal voltage from the plurality of input terminals to the plurality of thin film transistors, at least a portion [thereof] of one of said wires having a lamination structure comprising two or more conductive layers formed of two or more layers used to form the thin film [transistor] transistors, the portion of the wire being located near the peripheral area of the substrate and outside of said plurality of thin film transistors to function as an electric shielding wire.

3. (Twice Amended) A display apparatus having a plurality of pixels, comprising on a substrate:

a plurality of pixel electrodes corresponding to respective pixels among the plurality of pixels;

a plurality of switching thin film transistors, each comprising a plurality of conductive layers, connected to the plurality of pixel electrodes, for supplying signal voltage to the plurality of pixel electrodes;

a plurality of driving thin film transistors, each comprising a plurality of conductive layers, arranged close to peripheral area of the plurality of pixel electrodes, for generating a driving signal for driving [the] a number of switching thin film transistors;

a plurality of input terminals for receiving a control signal for driving the plurality of driving thin film transistors; and

wires, at least some of said wires [for] connecting the plurality of driving thin film transistors and the plurality of input terminals, at least a portion [thereof] of one of said wires having a lamination structure comprising two or more conductive layers formed of two or more layers included in each switching thin film transistor and/or each driving thin film transistor, the portion of the wire being located near the peripheral area of the substrate and outside of said plurality of driving thin film transistors to function as an electric shielding wire.

15. (Amended) A display apparatus having a plurality of pixels, comprising on a substrate:

a plurality of pixel electrodes corresponding to respective pixels among the plurality of pixels;

a plurality of thin film transistors, each located outside of said plurality of pixel electrodes and comprising a plurality of conductive layers, for controlling supplying of signal voltage to the plurality of pixel electrodes;

a plurality of input terminals for receiving a control signal for the signal voltage to be supplied to the plurality of thin film transistors; and

wires, at least some of said wires being connected between said plurality of thin film transistors and said plurality of input terminals for sending the signal voltage from the plurality of input terminals to the plurality of thin film transistors, [at least a portion thereof having a lamination structure comprising two or more conductive layers formed of two or more layers used to form the thin film transistor,] wherein each of the wires includes a first conductive layer formed of the lowest conductive layer of the thin film transistor and a second conductive layer situated above the first conductive layer and formed of other conductive layer of the thin film transistor, at least a portion of one of said wires being located near the peripheral area of the substrate and outside of said plurality of thin film transistors to function as an electric shielding wire.